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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/570,290 | 02/28/2006 | Adrianus Josephus Bink | NL031031 | 5446 |

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| EXAMINER | |
|---|---|
| GIARDINO JR, MARK A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2185 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 03/13/2008 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/570,290 | BINK ET AL. | |
| | Examiner | Art Unit | |
| | MARK A. GIARDINO JR | 2185 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *21 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/28/2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## ***DETAILED ACTION***

The Examiner acknowledges the applicant's submission of the amendment dated 12/21/2007. At this point, claims 1-8 have been amended and claims 9-11 have been added. Thus, claims 1-11 are pending in the instant application.

The instant application having Application No. 10/570,290 has a total of 11 claims pending in the application, there are 2 independent claims and 9 dependent claims, all of which are ready for examination by the examiner.

## REJECTIONS BASED ON PRIOR ART

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4, 5, and 7-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Emma et al (US 5,584,002).

**Regarding Claim 1**, Emma teaches an integrated circuit, comprising:

at least one processing unit (Processor 340 in Figure 5);

a cache memory having a plurality of memory modules for caching data (Cache Unit 300 in Figure 5);

remapping means for performing an unrestricted remapping within said plurality of memory modules (inherently present to remap the data from one congruence class to another congruence class, Column 3 Lines 54-58), wherein the unrestricted remapping permits remapping the memory modules from a first bank of memory modules (each bank corresponds to a congruence class in Emma, Column 1 Lines 38-41) to a second bank of memory modules (Column 3 Lines 54-58, when the data is remapped from a first congruence class to a second congruence class, it is the equivalent of going from a first bank to a second bank).

**Regarding Claim 2**, Emma teaches the integrated circuit according to Claim 1, wherein said cache memory is a set-associative cache (Column 8 Lines 20-22).

**Regarding Claim 4,** Emma teaches the integrated circuit according to Claim 1, wherein said remapping means is adapted to perform the remapping on the basis of a reduction mapping (Column 9 Lines 5-18, where the remapping means must take as input the congruence and synonym class parameters but only output the identification (AMID) bits, therefore there are fewer output symbols than input symbols).

**Regarding Claim 5**, Emma teaches all limitations of Claim 1, further comprising:

a Tag RAM unit associated to said cache for identifying which data is cached in said cache memory (included in Cache Directory 310 of Figure 5, the AHIGH field 307 acts as a tag);

wherein said remapping means is arranged in series with said Tag RAM unit (Column 9 Lines 5-18, since the remapping is done at power-on, the remapping is done

prior to any checking of the Tag RAM, thus the remapping and Tag RAM are arranged serially).

**Regarding Claim 7,** Emma teaches all limitations of Claim 5, further comprising a look up table for marking faulty memory modules (Column 9 Lines 9-11, the SC bit of each cache entry acts as a look up table for each faulty module).

**Regarding Claim 8**, Emma teaches a method of cache remapping in an integrated circuit having at least one processing unit (processor 340 in Figure 5); a main memory for storing data (present between the cache and processor, Column 2 Lines 42-44); and a cache memory having a plurality of memory modules for caching data (caching unit 300 in Figure 5), the method comprising:

performing an unrestricted remapping within said plurality of modules, wherein the unrestricted remapping permits remapping the memory modules from a first bank of memory modules to a second bank of memory modules (Column 3 Lines 54-58, when the data is remapped from a first congruence class to a second congruence class, it is the equivalent of going from a first bank to a second bank).

**Regarding Claim 9,** Emma teaches all limitations of Claim 1, wherein the remapping means is further configured to distribute faulty memory modules evenly over a plurality of banks (Column 9 Lines 5-18, where alternate congruence classes are selected among synonym classes, thus a fault in a particular bank is mapped to a particular synonym class, and a fault from a different bank would be mapped to a different synonym class, thereby evenly distributing the faults, also see how each congruence class is assigned a synonym class, Column 3 Lines 26-35).

**Regarding Claim 10,** Emma teaches all limitations of Claim 1, wherein the remapping means is further configured to perform an unrestricted remapping at a block/line granularity level of modules (Emma teaches remapping at a line granularity, Column 3 Lines 33-35).

**Regarding Claim 11,** Emma teaches the integrated circuit according to Claim 1, wherein the remapping means is further configured to remap at least one of the memory modules from an index to a different index (Column 5 Lines 5-18, the remapping is done by remapping the AMID field [corresponding to the cache index] in a different congruence class).

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**Claim 3** is rejected under U.S.C. 103(a) as being unpatentable over Emma in view of Asher (US 6,671,822).

**Regarding Claim 3**, Emma teaches all limitations of Claim 1 as described above. However, Emma does not teach a programmable permutation means for remapping. Asher teaches remapping means adapted to perform the remapping on the basis of a programmable permutation function (see bus 18 in Figure 2, which uses a

multiplexer to permute way 0 to another given way; it is the multiplexer select bits that enable this permutation mapping to be programmed). It would have been obvious to a person of ordinary skill in the art to which the subject matter pertains at the time the invention was made to have used programmable permutation functions instead of a reduction mapping, since programmable permutation functions allow for greater flexibility in choosing which line to remap to (Column 6 Lines 21-22 in Asher).

**Claim 6** is rejected under U.S.C. 103(a) as being unpatentable over Emma in view of Kramer (US 4,868,869).

**Regarding Claim 6**, Emma teaches all limitations of Claim 1 as been discussed above. However, Emma does not teach a Tag RAM in parallel with said remapping means. Kramer teaches several lookup tables and additional circuitry (which is what a Tag RAM unit and a remapping unit with Map RAM are) connected in parallel (see Figure 9 in Kramer). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains to have placed the Tag RAM and remapping means of Emma in parallel as taught by Kramer. As motivation, connecting circuitry in parallel generally leads to a faster circuit. Thus, by putting the units in parallel, additional benefits are obtained. Also, parallel remapping means al

**ARGUMENTS CONCERNING NON-PRIOR ART REJECTIONS/OBJECTIONS**

***Drawing Objections***

Applicant's arguments, filed 12/21/2007, with respect to the drawings on Pages 12-13 have been fully considered and are persuasive. The objection to the drawings has been withdrawn.

***Specification Objections***

Applicant's arguments/amendments with respect to the specification have been considered and have overcome the Examiner's prior objections and thus are withdrawn.

***Rejections - USC 112***

Applicant's arguments/amendments with respect to Claim 4 have been considered and have overcome the Examiner's prior rejections and thus are withdrawn.

**ARGUMENTS CONCERNING PRIOR ART REJECTIONS**

***Rejections - USC 102/103***

Applicant's arguments, see pages 15-17, filed 12/19/2007, with respect to the rejection(s) of claim(s) 1-8 in view of Lefsky and Asher, are moot in view of new ground(s) of rejection made in view of Emma (US 5,584,002), which was cited by the examiner on the Office Action dated 9/21/2007.

Applicant's argument on Page 13 that there was no rejection to Claim 6 has been considered, but it is not persuasive. The scope of the Claim has changed, and new grounds of rejection are necessary in response to Applicant's amendment.

**CLOSING COMMENTS**

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

**STATUS OF CLAIMS IN THE APPLICATION**

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

**CLAIMS REJECTED IN THE APPLICATION**

Per the instant office action, claims 1-11 have received a second action on the merits and are subject of a second action final.

**DIRECTION OF FUTURE CORRESPONDENCES**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Anthony Giardino whose telephone number is (571) 270-3565 and can normally be reached on Monday - Thursday 7:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571) 272 - 4098. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M.A. Giardino

/M.G./

Patent Examiner
Art Unit 2185

March 11, 2008

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185